CLAIMS:

1. A composite substrate comprising a carrier composed of a carrier material, a first layer composed of a first material, and an intermediate layer composed of a second material being located between the carrier and the first layer, wherein the first material has a dilatation behavior being substantially the same as that of the carrier material, and having a dilatation mismatch with the second material, the intermediate layer having structures of second material for absorbing stress originating from the dilatation mismatch.

2. A composite substrate according to claim 1, wherein the intermediate layer has a thickness, and the structures extend through the thickness of the intermediate layer.

3. A composite substrate according to claim 1, wherein the structures further extend into the carrier.

4. A composite substrate according to claim 1, wherein the carrier material is the same as the first material.

5. A composite substrate according to any of the previous claims, wherein the carrier material and the first material are semiconductors.

6. A composite substrate according to any of the previous claims, wherein the second material is an electrically insulating material.

7. A composite substrate according to any of the previous claims, the intermediate layer lying in a plane, wherein the dimensions of the structures in the plane of the intermediate layer are less than a centimeter.

8. A composite substrate according to any of the previous claims, wherein the carrier lies in a plane and wherein the structures have a line-symmetric shape in a cross-section perpendicular to the plane of the carrier.

9. A composite substrate according to any of the previous claims, wherein the carrier lies in a plane and wherein the structures have a circular, square, rectangular or rhombic shape in a cross-section parallel to the plane of the carrier.

10. A composite substrate according to any of the previous claims, wherein the composite substrate is a silicon-on-insulator wafer.

11. A method to relieve stress in a composite substrate, comprising:

providing a carrier, composed of a carrier material, with on top thereof an intermediate layer of a second material,

forming in the intermediate layer structures which extend through the intermediate layer,

bonding on the intermediate layer a first substrate of a first material having a dilatation behavior being substantially the same as that of the carrier material.

12. A method according to claim 11, in which the structures are formed into the carrier.

13. A method according to claim 11 or 12, wherein the forming of the structures is executed by integrally patterning the structures over the intermediate layer.

14. A method according to claim 11 or 12, wherein the forming of the structures is executed by locally patterning the structures in clusters over the intermediate layer.

15. A method according to any of claims 11 to 14, wherein the patterning comprises applying millimeter, micrometer or nanometer structural texturing.

16. A method according to any of claims 11 to 14, wherein the patterning comprises applying imprint lithography.

17. A method according to any of claims 11 to 16, wherein the intermediate layer lies in a plane, and wherein the forming of the structures is such that the dimensions of the structures in the plane of the intermediate layer are less than a centimeter.

18. A method according to any of claims 11 to 17, wherein the carrier lies in a plane, and wherein the forming of the structures is such that the structures have a line-symmetric shape in a cross-section perpendicular to the plane of the carrier.

19. A method according to any of claims 11 to 18, wherein the carrier lies in a plane, and wherein the forming of the structures is such that the structures have a circular, square, rectangular or rhombic shape in a cross-section parallel to the plane of the carrier.

20. Use of the method of any of claims 11 to 19 for making a silicon-on-insulator substrate.